AMENDMENTS TO THE SPECIFICATION

In the specification, page 24, please replace paragraph [0057], with the following amended paragraph:

A planation film 31 is formed on the aforementioned semiconductor substrate 1. For example, the planation film 31 is formed by sequentially laminating a silicon oxide film of 300 nm thickness by way of the plasma CVD (plasma chemical vapor deposition) method, as SOG film of 600 nm thickness, ~~and a silicon oxide film of 50 nm thickness composed of triethoxy silane~~ and a silicon oxide film of 50 nm thickness, which is formed by way of the plasma CVD method using the TEOS method, thus forming a planar insulating film.

In the specification, pages 25 and 26, please replace paragraph [0061], with the following amended paragraph:

[0061]

Next, as shown in FIG. 10(b), a resist film 36 of 3 μm thickness is formed on the overall surface of the thick film 35. Thereafter, prescribed parts of the resist film 36 are removed by way of ~~etching~~ exposure and development, thus forming a prescribed resist pattern. Thus, channel regions are exposed with respect to the via A, pad B, and channel forming region C.

In the specification, pages 32, 33 and 34, please replace paragraphs [0084], [0085], [0086], [0087] and [0088] with the following amended paragraphs:

[0084]

Next, as shown in FIG. 18(b) a mold 37 137 is attached to a contact aligner (not shown); then, the semiconductor substrate 1 in which the resist film 36 is formed is positioned at a prescribed position of the contact aligner, so that the mold ~~37~~ 137 is positioned opposite to the resist film 36 formed on the semiconductor substrate 1. In this case, positioning is performed between alignment marks, which are applied to the semiconductor substrate 1, and alignment marks, which are applied to the mold ~~37~~ 137 at prescribed positions opposite to the semiconductor substrate 1, thus establishing precise positioning between the semiconductor substrate 1 and the mold ~~37~~ 137.

[0085]

The mold ~~37~~ 137 is composed of quartz, in which the aforementioned alignment marks are applied at the prescribed positions opposite to the semiconductor substrate 1. In addition, a plurality of projections ~~37a~~ 137a, which are consecutively aligned in a zigzag manner (and whose cross sections are each formed in an acute triangular shape having a summit), are formed in the mold ~~37~~ 137 at prescribed positions suiting the channel forming regions C of the thick film 35.

[0086]

Next, as shown in FIG. 18©, the mold ~~37~~ 137 is pressed against the resist film 36 formed on the semiconductor substrate 1. In order to realize easy separation between

the resist film 36 and the mold ~~37~~ 137 in the after-treatment, it is preferable that the contact surface (particularly, the lower surface at which the projections ~~37a~~ 137a are formed) of the mold ~~37~~ 137 in contact with the resist film be covered with a fluorocarbon resin or be subjected to prescribed surface processing (or silicon processing).

[0087]

Thereafter, the resist film 36 is subjected to heat treatment for ten minutes at a temperature of 150°C, thus dissolving the resist film 36. This makes the terminal surfaces of the via A and the pad B be inclined; and channels suiting the projections ~~37a~~ 137a are formed in the channel forming region C.

Incidentally, as the temperature is increased from the room temperature, the resist film 36 becomes softened at 150°C, and then it becomes hardened when the temperature of 200°C. That is, the resist film 36 is not hardened at the temperature of 150°C. In the present embodiment, the mold ~~37~~ 137 is subjected to pressing as the resist film 36 becomes softened, so that the channel forming region C is deformed in shape to suit the projections ~~37a~~ 137a. Next, while the mold ~~37~~ 137 is being pressed against the resist film 36 on the semiconductor substrate 1, the resist film 36 is cooled, and then the mold ~~37~~ 137 is separated, so that the resist film 36 is hardened without changing channel shapes formed therein. When the heating temperature exceeds 100°C, solvent starts to be vaporized, thus improving adhesion between the semiconductor substrate 1 and the resist film 36.

[0088]

Next, as shown in FIG. 18(d), the mold ~~37~~ 137 is separated from the resist film 36. This allows the channels 36a whose shapes suit the projections ~~37a~~ 137a of the mold ~~37~~ 137 to be formed in the resist film 36. Incidentally, the aforementioned mold ~~37~~ 137 can be combined with a photomask; hence, it is possible to simultaneously realize the pattern formation of the resist film 36 and the formation of the channels 36a.

In the specification, page 37, please replace paragraph [0100], with the following amended paragraph:

[0100]

According to the manufacturing method of the magnetic sensor of the present embodiment, it is possible to form the X-axis sensor 2, Y-axis sensor 3, and Z-axis sensor 4 on a single semiconductor substrate 1 and to also form the via A and the pad B; it is possible to easily produce a small-size three-axial magnetic sensor by way of a series of consecutive processes. In addition, the mod ~~37~~ 137 having the projections ~~37a~~ 137a, which are shaped to suit the channels 8 formed in the thick film 35, is pressed against the resist film 36 so as to form the channels 8; hence, it is possible to easily form the channels 8 by way of the etching of the thick film 35. This improves the planation with respect to the slopes of the channels 8. Since the magneto-sensitive elements forming the giant magnetoresistive elements are formed on the slopes of the channels 8, it is possible to form the Z-axis sensor 4 having a fixed sensing direction and a high sensitivity.

In the specification, on page 45, please replace paragraph [0123]with the following amended paragraph:

[0123]

Next, the manufacturing method of the magnetic sensor of the fourth embodiment will be described.

First, similar to the first embodiment, the foregoing processes shown in FIGS. 9(a) to (d) are performed. Then, as shown in FIG. 26(a), the insulating film 37 of 0.2 μm thickness is formed by way of sputtering. The insulating film 37 is composed of aluminum oxide (Al_2O_3), boron nitride (BN), and diamond-like carbon. As the insulating film, it is possible to use one such as a silicon nitride film and a silicon oxide film having an etching rate lower than that of the thick film 35.

In the specification, please replace page 46, paragraph [0126]with the following amended paragraph:

[0126]

Next, as shown in FIG. 28(a), the thick film 35 of 5μm thickness composed of silicon oxide is formed by way of the plasma CVD method. [[A]] Then a plurality of the channels 8 are formed in the thick film 35.